Subst. Form PTO-1449 APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: RPS920010172US1 (IRA-10-5709)	Serial No.: To be assigned
	Applicant: Atoji et al	
	Filing Date: Herewith	Group: ~~To be assigned~~ 2193

U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
MPF	AA	5,815,688	09/29/1998	Averill	395	500	10/09/1996
MPF	AB	5,646,949	07/08/1997	Bruce, Jr. et al	37	127	06/04/1996
MPF	AC	5,572,666	11/05/1996	Whitman	395	183.08	03/28/1995
MPF	AD	5,488,573	01/30/1996	Brown et al	364	578	09/02/1993
MPF	AE	5,455,938	10/03/1995	Ahmed	364	488	09/14/1994
MPF	AF	5,210,861	05/11/1993	Shimoda	395	575	05/30/1990
MPF	AG	4,984,239	01/08/1991	Suzuki et al	371	3	01/04/1989
	AK						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subcl.	Translation?
MPF	AL	JP2001051965A	08/12/1999	Japan	—	—	No
MPF	AM	JP11232131A	02/13/1998	Japan	—	—	No
MPF	AN	JP11230160A	01/16/1998	Japan	—	—	NO
MPF	AO	JP10187475A	12/25/1996	Japan	—	—	No
MPF	AP	JP8166892A	12/13/1994	Japan	—	—	No
MPF	AQ	JP01180645	01/13/1988	Japan	—	—	No

OTHER DOCUMENTS

MPF	AR	"A Biased Random Instruction Generation Environment for Architectural Verification of Pipelined Processors", Journal of Electronic Testing: Theory and Applications, pgs. 13-27 (2000), Ta-Chung Chang
MPF	AS	"Micro Architecture Coverage Directed Generation of Test Programs", Design Automation Conference, June 21-25, 1999, pgs. 175-180
MPF	AT	"Verification by Behavorial Modeling – A Multiprocessor System Case, Conference on ASIC Proceedings", October 21-24, 1996, pgs 43-45
MPF	AU	"Automatic Test Program Generation for Pipelined Processors", IEEE/ACM International Conference on CAD-94, November 6-10, 1994, pgs. 580-583

Examiner: Mark P. Francis | Date Considered: 7/6/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP 609; draw line through citation if in conformance and not considered. Include copy of this form with next communication to applicant.